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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,313	01/18/2002	Robert L. Hodges	10004054 -1	8400

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,313	HODGES ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13 and 19-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 19-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hsien Ming Lee 7/13/2004

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Claims 7-13 and 19-33are pending in the application. The indication of allowable subject matter to claims 24-31 is withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The added limitation "and is electrically isolated by the deposited layer of oxide" (lines 16-17) is not clear as to whether the gate electrode is isolated or active areas are isolated.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 24 and 26-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. (US 6,200,862).

In re claims 24, 29 and 30, Gardner et al. teach a method of making a semiconductor device comprising:

- depositing a layer of oxide 40 proximate a first surface of a semiconductor substrate 10 (Fig.2C);
- exposing a portion of the first surface (i.e. top surface) of the semiconductor substrate 10 (Fig.2A);
- forming a gate oxide layer 22 on the exposed portion of the first surface, adjacent to the deposited oxide layer 40 (Fig.2C);
- forming a pair of active areas 28/34 in the exposed portion of the first surface adjacent to the deposited oxide layer 40 and the gate oxide layer 22 (Fig.2C);
- forming a gate electrode 24 by depositing a conductive layer (polysilicon, col. 3, lines 57-58) over the gate oxide layer (Fig.2A);
- deposing a dielectric layer 46 (silicon dioxide, col. 4, lines 62-63) over the gate electrode 24, active areas 28/34 and deposited oxide layer 40 (Fig.2C); and
- forming electrical contacts 42/44 to the pair of active areas 28/34 and the gate electrode 24 (Fig.2C).

In re claim 26, Gardner et al also teach that the semiconductor substrate 10 is P-type silicon (i.e. doped with P-type dopant, boron, col. 3, line 30).

In re claims 27 and 28, Gardner et al. teach that the active areas 28/34 are formed by impurity implant (col. 4, lines 27-31); and the active areas 28/34 are n doped regions because the active areas are implanted with opposite-type ions as compared to substrate 10, which is P-type (col. 4, lines 2-6).

In re claim 31, Gardner also teaches a semiconductor device produced by the method of claim 24.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7, 9-13 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner (US 6,200,862) in view of Bhaskar et al. (US 5,635,968).

In re claims 7, 9, and 12, Gardner et al. teach the claimed method (Fig. 2A-2C), comprising:

- depositing a layer of oxide 40 proximate a first surface (i.e. a top surface) of a semiconductor substrate 10 (p-type silicon, col.3, lines 24-31);
- forming a gate oxide layer 22 on the first surface, adjacent to the deposited oxide layer 40;
- forming a pair of active areas 28/34 in the first surface, adjacent to the deposited oxide layer 40 and gate oxide layer 22 because active areas 28/34 are right under the deposited oxide layer 40 and active areas 28/34 are also proximate to the gate oxide layer 22 with at least a point contact (Fig.2B);
- forming a gate electrode 24 by depositing a conductive layer (polysilicon, col.3, lines 57-58) over the gate oxide layer 22 (Fig.2A);

- depositing a dielectric layer 46 over the gate electrode 24,active region 28/34, and deposited oxide layer 40 (Fig.2C); and
- forming electrical contacts 44 to the pairs of active areas 28/34 and the gate electrode 24.

Gardner et al. do not teach forming the pair of active areas 28/34 after depositing the layer oxide.

Bhaskar et al., in an analogous art, teach forming the oxide layer 903 by CVD (Fig.9); forming an opening in the oxide layer 903 and then forming the active areas 907 and 911.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to modify Gardner's method by applying the teachings of Bhaskar et al so that the active areas 28 and 34 is formed after depositing the oxide layer and forming the opening in the oxide layer, since by this manner it would precisely control a desired location for forming the active areas.

In re claim 10, Gardner et al. also teach that the active areas 28/34 are formed by impurity implant and diffusion, i.e. forming source/drains (col.4, 5-30).

In re claim 11, Gardner et al. also teach that the active areas 28/34 are n-doped regions when channel is p-type (col. 3, lines 30-31 and col.4, lines 2-5).

In re claim 13, Gardner et al. also teach that the dielectric layer 46 is silicon dioxide (col. 4, lines 62-63).

In re claim 32, Gardner et al. also teach a semiconductor device (i.e. a insulated gate transistor or IGFET) produced by the method of claim 7.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. in view of Bhaskar et al as applied to claim 7 above, and further in view of Liu et al (US 2003/0081070).

Gardner et al. in view of Bhaskar et al. teach all limitations, as stated above, but do not teach thermally growing a thermal oxide layer before depositing the layer of oxide on the first surface of the semiconductor substrate.

However, Liu et al., in an analogous art, teach thermally growing a thermal oxide layer 32 before depositing the layer of oxide 36 on the first surface of the semiconductor substrate 25 (Figs 3A-3B).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to thermally grow the oxide, as taught by Liu et al, before depositing the oxide layer of Gardner et al., since by doing so it would provide a better electrical insulation for adjacent layers.

9. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhaskar et al. (US 5,635,968) in view of Tseng (US 2002/0058368).

Bhaskar et al., in Figs. 9-13 and related text, teach a method of forming a semiconductor device (i.e. a thermal inkjet print head) comprising:

- depositing a layer of oxide 903 (i.e. a CVD-deposited silicon dioxide, col. 10, lines32-34) proximate a first surface (i.e. top surface) of a semiconductor substrate 901(Fig.9);
- exposing a portion (i.e. an opening as shown in Fig. 9) of the first surface of the semiconductor substrate 901; and

- forming a field effect transistor (i.e. FET) 905 on the exposed portion of the first surface of the substrate having the deposited oxide layer 903, wherein said FET 905 includes a gate electrode 909 with associated active areas 907 and 911 and FET 905 is electrically isolated by the deposited layer of oxide 903.

Bhaskar et al. are silent as to the associated active areas 907 and 911 are formed after the exposing in the first surface of the semiconductor substrate 901. However, it would have been obvious to one of the ordinary skill in the art to comprehend that the active areas 907 and 911 are formed by ion implantation after exposing the first surface (i.e. top surface) of the substrate by forming an opening in the oxide layer 903. Without firstly forming the opening in the oxide layer 903 it is impossible to form the active areas 907 and 911, as evidenced by Tseng.

Tseng, in an analogous art of forming FET, teaches forming a deposited oxide 48 on the substrate 42 (Fig.2A); exposing a first surface (i.e. top surface) of the substrate 42 via a formation of a trench 51 (Fig.2B); and forming active area 52 (i.e. impurity region) by ion implanting through the trench 51 after exposing the first surface (Fig.2B).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to comprehend that the active areas in Bhaskar et al. are formed after exposing the first surface of the substrate, since without forming the opening in the oxide layer to expose the surface of the substrate it is impossible to form the active areas, as evidenced by Tseng.

10. Claim 19-21 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhaskar et al.(US '968) in view of Saul (US 6,318,846).

In re claims 19-21, Bhaskar et al., in Figs. 11-13 and related text teach the claimed method of manufacturing a semiconductor device (i.e. a thermal inkjet print head) comprising:

- depositing a current prevention layer 1201 proximate a first surface of a semiconductor substrate 103/1101 (Fig. 11); and
- forming a field effect transistor (i.e. FET) 905, wherein said FET includes a gate electrode 909 with associated active areas 907 and 911 formed in the first surface of the semiconductor substrate 103/1101 having the deposited current prevention layer 1201 thereon; and forming a firing chamber 1307 above the current prevention layer 903 (Fig.13).

In contrast, Bhaskar et al. teach a single transistor 905 but do not teach plural transistors including a first FET and a second FET, wherein the current prevention layer includes a region that minimizes current flow between the active areas of the first FET with respect to the active area of the second FET.

Saul, in an analogous art of forming a thermal inkjet print head, teach forming a plurality of FETs, which at least includes a first and a second FETs and the FETs share a common ground and have their source coupled to V+ through a corresponding heater resistor, on a substrate for the purpose of improving reliability of the print head (col. 5, lines 21-35 and 48-64; col. 10, lines 6-15; col. 11, lines 5-17 and 35-47 and col. 12, lines 49-52).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to modify the method of Bhaskar et al in a manner suggested by Saul so that plural FETs, at least including the first and second FETs, are

formed on the substrate in a such way that the first and second FETs are separated by the current prevent layer (i.e. a dielectric layer) and the current flow between the active areas (i.e. first source/drain regions) of the first FET with respect to the active areas (i.e. second source/drains regions) of the second FET can be minimized due to the presence of the dielectric layer between two FETs.

The motivation/suggestion for doing so would be to improve the reliability of the print head (col. 5, lines 59-64, Saul).

In re claim 33, Bhaskar et al. in view of Saul also teach the claimed fluid ejection device (i.e. thermal ink jet print head) produced by the method of claim 19.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (US '862) in view of Liu et al (US '070).

Gardner et al. do not teach thermally growing a thermal oxide layer before depositing the layer of oxide.

However, Liu et al., in an analogous art, teach thermally growing a thermal oxide layer 32 before depositing the layer of oxide 36 on the first surface of the semiconductor substrate 25 (Figs 3A-3B).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to thermally grow the oxide, as taught by Liu et al, before depositing the oxide layer of Gardner et al., since by doing so it would provide a better electrical insulation for adjacent layers.

Response to Arguments

12. Applicant's arguments filed 4/29/04 have been considered but are moot in view of the new ground(s) of rejection.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

July 13, 2004

Hsien Ming Lee
7/13/2004